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Customer No.: 31561  
Application No.: 10/707,082  
Docket No.: 11690-US-PA

**REMARKS****Present Status of the Application**

Claims 1-14 remain pending of which claims 1, 5 and 7 have been amended and claims 12-14 have been newly added to more clearly describe the claimed invention. Amendments to claims are fully supported at paragraphs [0031]-[0034]. Therefore, it is believed that no new matter adds by way of amendment to claims or otherwise to the application.

For at least the following reasons, Applicant respectfully submits that claims 1-14 are in proper condition for allowance. Reconsideration is respectfully requested.

**Discussion of the claim rejection under 35 USC 102**

*The Office Action rejected claims 1, 2, 5 and 7 under 35 U.S.C. 102(e) as being anticipated by Sakimura et al. (US-6,885,579, hereinafter Sakimura).*

Applicants respectfully disagree and submit that it is well established that under 35 U.S.C. 102, each and every elements of the rejected claim must be exactly disclosed by a single prior art reference.

Applicants respectfully submit that Independent claim 1, as amended, recites, among other things, [a sensing amplifier; and a switch device coupled to the memory cell, a power supply terminal, the sensing amplifier, the column selection line and the row selection line, wherein when both the column selection line receives a column turn-off signal and the row selection line receives a row turn-off signal, the switch device is

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turned off so that a power provided from the power supply terminal is not coupled to the memory cell].

Applicants respectfully submit that no where in Sakimura there is any disclosure regarding a sensing amplifier connected to a switch device coupled to the memory cell. Therefore, Sakimura cannot possibly teach or anticipate the proposed amended claim 1 in this regard.

Furthermore, Applicants respectfully submit that the proposed Independent claim 5, as amended, recites, among other things, [selecting a column in response to a memory cell within a memory array; selecting a row in response to the memory cell within the memory array; and coupling a column turn-off signal to the column and a row turn-off signal to the row when it is determined that the memory cell is defective and so that a power provided from a power supply terminal is not coupled to the memory cell]. The advantage of the above features is that at least not only the problems due to current leakage in the memory cell are resolved but also reduction of service life of the batteries, slowing down of operating speed of the memory devices, increase in operating temperature of the computer.

Applicants would like to point out that Sakimura teaches a method/device for restraining parasitic electric current (or sneak path electric current) in a MRAM in order to improve the reliability of determining data stored in a memory cell in a MRAM adopting a cross point cell array. However, no where in Sakimura's disclosure there is any device or method for repairing defective memory cells. Therefore, Sakimura cannot possibly teach or anticipate any method for breaking a leakage current path in a memory

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array within a memory device, comprising at least [selecting a column in response to a memory cell within a memory array; selecting a row in response to the memory cell within the memory array; and coupling a column turn-off signal to the column and a row turn-off signal to the row when it is determined that the memory cell is defective and so that a power provided from a power supply terminal is not coupled to the memory cell] as claimed in the amended claim 5.

In other words, Sakimura substantially teaches away from the claimed invention in this regard.

Therefore, Applicants respectfully submit that Sakimura cannot possibly anticipate the amended proposed independent claim 1 in this regard.

Because the proposed independent claim 7, as amended, also recite features that are similar to the amended proposed independent claim 1, therefore Applicants similarly submit that claim 7 also patentably defines over Sakimura for at least the same reasons discussed above.

Claims 2 and newly added claims 12-14, which directly depend from the independent Claims 1 and 7 are also patentable over Sakimura at least because of their dependency from an allowable base claim.

For at least the foregoing reasons, Applicants respectfully submit that claims 1, 2, 5, 7 and 12-14 patentably define over Sakimura. Reconsideration and withdrawal of above rejections is respectfully requested.

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**Discussion of the claim rejection under 35 USC 103**

1. *The Office Action rejected claims 4, 6, 10 and 11 under 35 U.S.C. 103(a) as being unpatentable over Sakimura in view Arimoto et al. (US-2003/0103368, hereinafter Arimoto).*

Applicants respectfully disagree and would like to point out that Arimoto substantially teaches a configuration in which a bit line precharge/equalize circuit is arranged in a sense amplifier band, a standby current can be likewise detected by disconnecting all non-selected memory cell arrays (memory blocks) from sense amplifier bands. In the sleep mode, by disconnecting a leakage-defective memory cell array from sense amplifier bands, a consumed current can be reduced even in a configuration in which a bit line precharge/equalize circuit is arranged in a sense amplifier band. As a configuration for control in such an arrangement, the configuration of control described above can be utilized. In other words, because Arimoto substantially fails to teach, suggest or hint disconnecting the power supply to the selected defective memory cell, instead Arimoto substantially teaches disconnecting a leakage-defective memory cell array from sense amplifier bands. Accordingly, even if the above features of the Arimoto were to be incorporated into Sakimura in a manner suggested by the Examiner, still the combination cannot possibly render every features of the claimed invention for at least the reasons discussed above.

For at least the foregoing reasons, Applicants respectfully submit that claims 4, 6, 10 and 11 patently define over Sakimura and Arimoto. Reconsideration and withdrawal of above rejections is respectfully requested.

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*2. The Office Action rejected claims 3 and 9 under 35 U.S.C. 103(a) as being unpatentable over Sakimura in view of Marr et al. (US-6,707,707, hereinafter Marr).*

Applicants respectfully disagree and submit that the PMOS transistor or PMOSFET transistor of Marr still cannot cure the specific deficiencies of Sakimura for at least the reasons substantially discussed above. Accordingly, Applicants respectfully submit that no combination of Sakimura and Marr in a manner suggested by the Examiner could possibly render every features of the claimed invention in this regard.

For at least the foregoing reasons, Applicants respectfully submit that claims 3 and 9 patently define over Sakimura and Marr. Reconsideration and withdrawal of above rejections is respectfully requested.

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**CONCLUSION**

For at least the foregoing reasons, it is believed that all pending claims 1-14 are in proper condition for allowance. If the Examiner believes that a conference would be of value in expediting the prosecution of this application, he is cordially invited to telephone the undersigned counsel to arrange for such a conference.

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Respectfully submitted,

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